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Tunable Gm-C Floating Capacitance Multiplier

Wipavan Narksarp and Yongyuth Naras
Department of Electrical Engineering,
Faculty of Engineering,
Siam University, Siam U
Bangkok, Thailand
E-mail: wipavan.nar@siam.edu,yongyuth.nar@siam.edu

Vinai Silaruam
Department of Telecommunication Engineering,
Faculty of Engineering,
Mahanakorn University of Technology, MUT
Bangkok, Thailand
E-mail: vinai@mut.ac.th

***Abstract*—In this article, a new tunable Gm-C floating capacitance multiplier is presented. It employs four simple transconductors and a grounded capacitor. The proposed capacitance multiplier offers the attractive features: simple configuration, electronically tunable capacitance multiplication factor, low sensitivities to variation of circuit elements and simple implementation of integrated circuit. The proposed floating capacitance multiplier using the transconductors with parasitic effects are examined. The performances of the proposed circuit and its application on band-pass filter are confirmed by using PSPICE simulation with 0.18 µm CMOS process parameter.**

Keywords— floating capacitance multiplier; grounded capacitor; transconductor; band-pass filter

I. INTRODUCTION

A capacitor is an important element in many circuit blocks such as filter, oscillator, and amplifier. In modern integrated circuit design, the fabricated implementation of high-valued capacitors is a major problem because of their large chip occupation. A possible solution of the problem is represented using the capacitance multiplication method. Thus, capacitance multipliers have received extensive attention. The capacitance multiplier employing several active building blocks such as second generation current conveyors (CCIIs) [1-2, 4, 5], operational amplifier (OPAMP) and operational transconductance amplifiers (OTAs) [3], current-controlled differential difference current conveyors (CCDDCCs) [6], voltage differencing buffered amplifier (VDBA) [7] and Current amplifier and DUA [8]. The circuit of [1-5] provides a grounded capacitance multiplier. However, a floating version of capacitance multiplier can provide wider applications than a grounded version. The floating capacitance multipliers have been reported [3-6]. The circuit of [5] requires two OTAs, an OPAMP, a voltage buffer, and an ungrounded capacitor. The circuit enjoys the attractive feature of electronic tuning of capacitance multiplication factor. But it might have the bandwidth and the slew rating problems on account of the OPAMP used and not attractive for integrated circuit implementation. Since the CCII gives several advantages, e.g., wider bandwidth, greater linearity and dynamic range over voltage-mode counterpart like OPAMP [9-10], it is very attractive for realization of the floating capacitance multiplier. The CCII-based floating capacitance multipliers have been proposed [4-5]. However, the floating capacitance multipliers do not offer electronic tunability. The new floating capacitance multiplier recently reported in [6] employs three CCDDCCs and a grounded capacitor. It provides the attractive features of electronic tuning of the capacitance multiplication factor and suitable for integration. Unfortunately, the circuit employs many transistors and consequently suffers from high power consumption and large chip area. Reference [7] has been proposed the tunable capacitance multiplier with a VDBA. It consists of one floating capacitor and an external resistor. Recently, [8] is presented the floating capacitance multiplier. However, the floating capacitor is employed in the same as [7].

In this paper, a novel circuit of floating capacitance multiplication using Gm-C is presented. It consists of sixteen MOS transistors as transconductors and a grounded capacitor. Its multiplication factor can be adjusted electronically by selecting the current bias of the transconductor. Since the circuit employs the grounded capacitor and no external resistor, its integrated circuit implementation is acceptable. The simulated characteristics of the floating capacitance multiplier and its application have been verified by PSPICE simulations.

II. CIRCUIT DESCRIPTION

A. Basic Circuit Configuration

The basic idea of the proposed capacitance multiplier is displayed in Fig. 1(a), consisting of five voltage-controlled current sources (VCCSs) and only one grounded capacitor. In Fig. 1(b), its equivalent circuit is shown. The current and voltage relations of node A and node B produce

$$V_A = \frac{sk_1C_1}{k_2k_3}(V_1 - V_2)\,. \tag{1}$$

Setting $k_4 = k_5$ gives

$$I_1 = k_4V_A\,, \tag{2}$$

and

$$I_2 = -k_4V_A\,. \tag{3}$$

Substituting (1) into (2) and (3) provides the short circuit admittance matrix as

$$[Y_1] = \frac{sk_1k_4C_1}{k_2k_3}\begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix}, \tag{4}$$

where k_i is the transconductance gain of the i^{th} VCCS. In (4), the basic circuit realizes a floating capacitance multiplier with the equivalent capacitance as

$$C_{eq} = \frac{k_1 k_4}{k_2 k_3} C_1 . \quad (5)$$

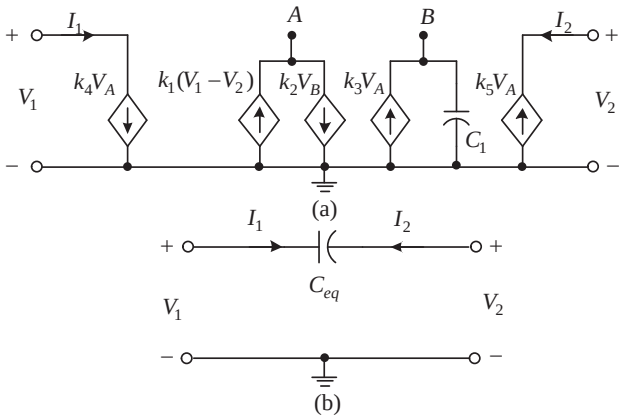

Fig. 1. (a) Proposed basic circuit, (b) its equivalent circuit.

It is noticed that the equivalent capacitance value is changed by the transconductance gains. The proposed floating capacitance multiplier based on G_m-C is described in the following section.

B. Proposed Floating Capacitance Multiplier

As previously discussed in the last section, the proposed capacitance multiplier employs the transconductors. Thus, the significant properties of the transconductor are briefly reviewed. Fig. 2 shows a simple transconductor based on four CMOS transistors and two bias current sources [11]. Assuming that these transistors have the same transconductance parameters and they also operate in the saturation region. The output currents of the transconductor yield

$$I_P = g_m V_I , \quad (6)$$

and

$$I_N = -g_m V_I , \quad (7)$$

where g_m is the transconductance of the transistor. It can be expressed as

$$g_m = (\mu_n C_{ox} \frac{W}{L} I_B)^{\frac{1}{2}} , \quad (8)$$

where I_B is the bias current of the transconductor, μ_n , C_{ox} and W/L are, respectively, the mobility of the electron carrier, the oxide capacitance and the aspect ratio of the transistor. Since the VCCSs of Fig. 1(a) substituted by the transconductor of Fig. 2, a new realization of the floating capacitance multiplier is presented in Fig. 3.

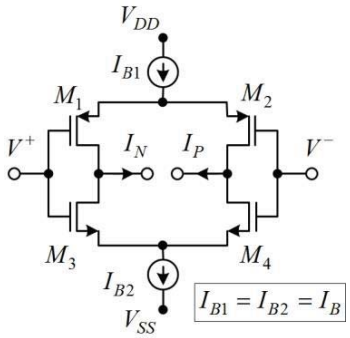

Fig. 2. Schematic of simple transconductor.

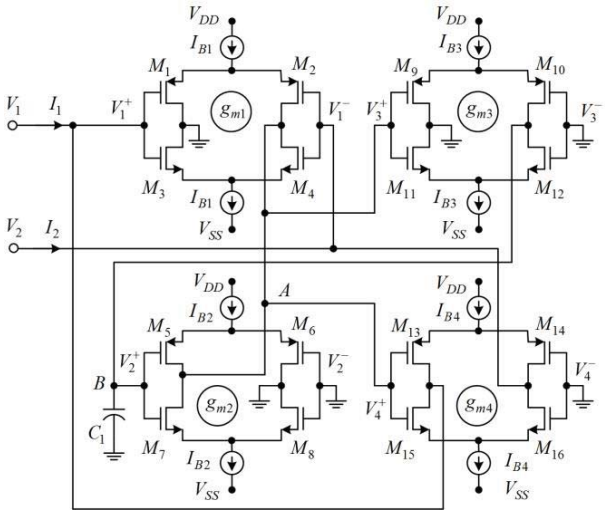

Fig. 3. Proposed floating capacitance multiplier.

This proposed circuit employs four transconductors and only one grounded capacitor. Routine analysis of this circuit yields the admittance matrix as

$$[Y_2] = \frac{s g_{m1} g_{m4} C_1}{g_{m2} g_{m3}} \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix}, \quad (9)$$

where g_{mi} is the transconductance value of the i^{th} transconductor. Comparison of (4) and (9) results $k_i = g_{mi}$, then the equivalent capacitance of the proposed circuit can be expressed as

$$C_{eq} = \frac{g_{m1} g_{m4}}{g_{m2} g_{m3}} C_1 . \quad (10)$$

From (10), the capacitance multiplication factor is given by

$$K = \frac{g_{m1} g_{m4}}{g_{m2} g_{m3}} . \quad (11)$$

Thus, the multiplication factor, K, can be electronically adjusted by varying the current I_B. The sensitivities of the equivalent capacitance with respect to circuit elements result the acceptably low values as follows:

$$S_{g_{m1}}^{C_{eq}} = -S_{g_{m2}}^{C_{eq}} = -S_{g_{m3}}^{C_{eq}} = S_{g_{m4}}^{C_{eq}} = S_{C_1}^{C_{eq}} = 1. \qquad (12)$$

C. High Frequency Consideration

From (9), the admittance matrix of the proposed circuit with ideal transconductor has been considered. For high frequency application, the transconductor with the parasitic elements affect the proposed circuit. Fig. 4 shows the equivalent circuit of the transconductor with the parasitic elements.

Considering these parasitic elements, the short circuit admittance matrix of the proposed circuit in Fig. 3 gives

$$[Y_3] = \begin{bmatrix} \dfrac{1}{Z_{X1}//Z_T} & -\dfrac{1}{Z_T} \\ -\dfrac{1}{Z_T} & \dfrac{1}{Z_{X2}//Z_T} \end{bmatrix}, \qquad (12)$$

where $Z_{X1} = \dfrac{1}{s(C_{I1+} + C_{N4}) + G_{N4}}$ $Z_{X2} = \dfrac{1}{s(C_{I1-} + C_{P4}) + G_{P4}}$

and $Z_T = \dfrac{g_{m2}g_{m3} + \Delta_T[s(C_1 + C_{I2+} + C_{P3}) + G_{P3}]}{g_{m1}g_{m4}[s(C_1 + C_{I2+} + C_{P3}) + G_{P3}]}$, where Δ_T is given by $\Delta_T = s(C_{P1} + C_{N2} + C_{I3+} + C_{I4+}) + G_{P1} + G_{N2}$.

Note that the terms of impedances $1/[s(C_{I1+}+C_{N4}) + G_{N4}]$ and $1/[s(C_{I1-} + C_{P4}) + G_{P4}]$ are effective at very high frequencies. The limitation at high frequencies is found to be

$$\omega << \min\left\{\frac{G_{P3}}{C_1 + C_{I2+} + C_{P3}}, \frac{G_{N4}}{C_{I1+} + C_{N4}}, \frac{G_{P4}}{C_{I1-} + C_{P4}}\right\}. \qquad (13)$$

It is seen from (14) that C_1 is selected as small as possible to increase the high frequency operation of the proposed circuit.

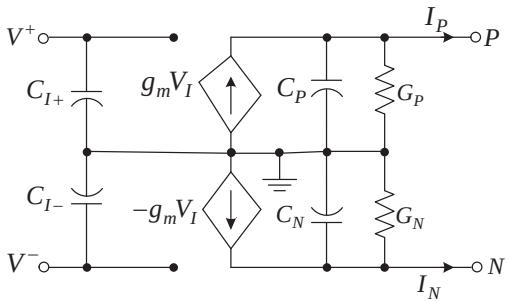

Fig. 4. Parasitic elements on the equivalent circuit of the transconductor.

III. Application Example

A. Second-order Band-pass Filter

To illustrate the proposed circuit application, the circuit is used to implement an active capacitor in a second-order band-pass filter (BPF) of Fig. 5 [12].

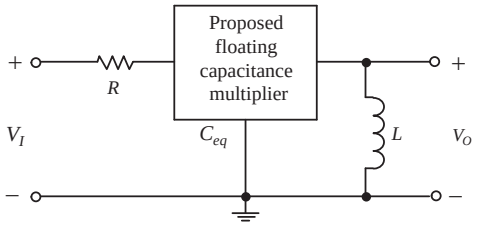

Fig. 5. Second-order band-pass filter.

The transfer function of the filter is expressed as

$$H_{BPF}(s) = \frac{s\dfrac{g_{m2}g_{m3}}{g_{m1}g_{m4}RC_1}}{s^2 + s\dfrac{g_{m2}g_{m3}}{g_{m1}g_{m4}RC_1} + \dfrac{g_{m2}g_{m3}}{g_{m1}g_{m4}LC_1}} \qquad (14)$$

From (14), center or resonant frequency ω_0, quality factor Q and bandwidth BW of the filter are given by

$$\omega_0 = \sqrt{\frac{g_{m2}g_{m3}}{g_{m1}g_{m4}LC_1}}, \; Q = R\sqrt{\frac{g_{m1}g_{m4}C_1}{g_{m2}g_{m3}L}}, \; BW = \frac{g_{m2}g_{m3}}{g_{m1}g_{m4}RC_1}.$$

The sensitivities of the filter parameters are found as

$$-S_{g_{m1}}^{\omega_0} = S_{g_{m2}}^{\omega_0} = S_{g_{m3}}^{\omega_0} = -S_{g_{m4}}^{\omega_0} = -S_L^{\omega_0} = -S_{C_1}^{\omega_0} = \frac{1}{2}, \qquad (15)$$

$$S_{g_{m1}}^{Q} = -S_{g_{m2}}^{Q} = -S_{g_{m3}}^{Q} = S_{g_{m4}}^{Q} = -S_L^{Q} = S_{C_1}^{Q} = 2S_R^{Q} = \frac{1}{2}, \qquad (16)$$

and

$$-S_{g_{m1}}^{BW} = S_{g_{m2}}^{BW} = S_{g_{m3}}^{BW} = -S_{g_{m4}}^{BW} = -S_R^{BW} = -S_{C_1}^{BW} = 1, \qquad (17)$$

which are very low value.

IV. Simulation Results

To verify the performance of the proposed floating capacitance multiplier in Fig.3, it has been simulated using PSPICE program based 0.18μm CMOS process with supply voltage of ±0.9 V. The parameters of the transistors are listed in [13] available from MOSIS. The aspect ratios (*W/L*) of the transistors are assumed of 3.6 μm/0.54 μm for NMOS and 9 μm/0.54 μm for PMOS. Fig. 6 shows impedance characteristics of the proposed circuit with different bias current of the first transconductor, I_{B1}. Similarly, the floating capacitances were simulated by adjusting I_{B1}. The results of the capacitances are shown in Fig. 7. They confirm that the simulated capacitance can be tuned by selecting the currents I_B of the transconductors.

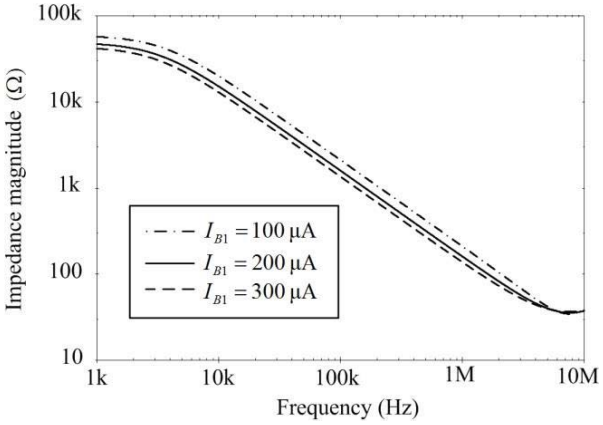

Fig. 6. Impedance characteristics of the circuit of Fig. 3 with different bias current.

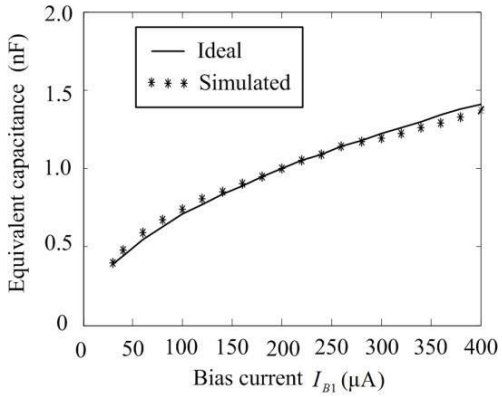

Fig. 7. Variation of the simulated capacitances versus ideal ones as the bias current is varied.

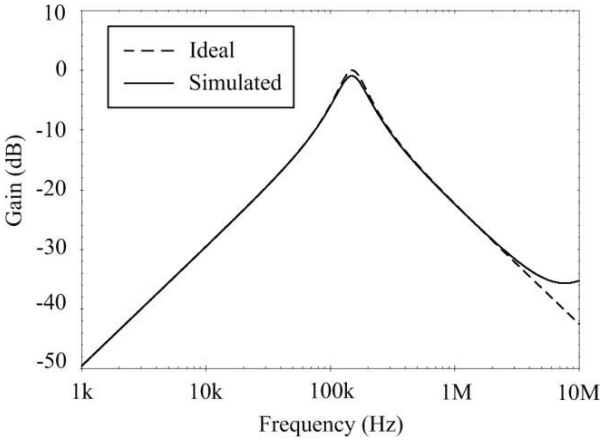

Fig. 8. Frequency responses of the BPF of Fig. 5.

For the example of BPF in Fig.5, it is designed on the 1nF proposed floating capacitance multiplier of Fig. 3 and passive elements of R = 2.13 kΩ and L = 1.13 mH, resulting in f_0 = 150 kHz, Q = 2, and BW = 469.48 kHz. The proposed capacitance multiplier is set as follows: I_{B1} = I_{B4} = 200 µA, I_{B2} = I_{B3} = 20 µA, and C_1 = 100 pF. The frequency responses of the BPF are depicted in Fig. 8. It should be noticed that the simulated result of the filter very closely approximates the theoretical one.

V. Conclusion

The new realization of the tunable floating capacitance multiplier is proposed in this paper. Its configuration is very simple. It employs only a grounded capacitor without another passive element, so the proposed capacitive multiplier is particularly attractive for IC implementation. Moreover, its multiplication factor can be electronically tuned by varying the bias current of the transconductor. The simulation results of the proposed tunable capacitance multiplier and its application show a good agreement with the expected results.

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